AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-12 (canceled).

13. (currently amended) A multi-level SONOS memory cell, comprising:

a substrate, comprising:

a substrate layer;

an insulation layer, disposed on the substrate layer;

a silicon stripe, disposed on the insulation layer;

a first control gate and a second control gate disposed respectively on sidewalls of the silicon stripe;

source/drain regions, configured in the silicon stripe beside both sides of the first control gate and the second control gate; and

a silicon oxide/silicon nitride/silicon oxide composite layer, disposed between the first control gate and the silicon stripe, and between the second control gate and the silicon stripe.

14. (original) The memory cell of claim 13, wherein the substrate comprises a silicon-on-insulator substrate.

15. (original) A multi-level memory cell, comprising:

a substrate;

an insulation layer, disposed on the substrate;

a semiconductive stripe, disposed on the insulation layer;

a first control gate and a second control gate disposed respectively on sidewalls of the semiconductive stripe;

source/drain regions, configured in the semiconductive stripe beside both sides of the first conductive gate and the second conductive gate;

a charge trapping layer, disposed between the first control gate and the semiconductive stripe, and between the second control gate and the semiconductive stripe;

a first dielectric layer, disposed between the charge trapping layer and the semiconductive stripe; and

a second dielectric layer, disposed between the charge trapping layer and the first control gate, and between the charge trapping layer and the second control gate.

16. (original) The multi-level memory cell of claim 15, wherein the semiconductive stripe comprises silicon.

17. (original) The multi-level memory cell of claim 15, wherein the charge trapping layer comprises a silicon nitride layer.

18. (original) The multi-level memory cell of claim 15, wherein the first dielectric layer comprises a silicon oxide layer.

19. (original) The multi-level memory cell of claim 15, wherein the second dielectric layer comprises a silicon oxide layer.